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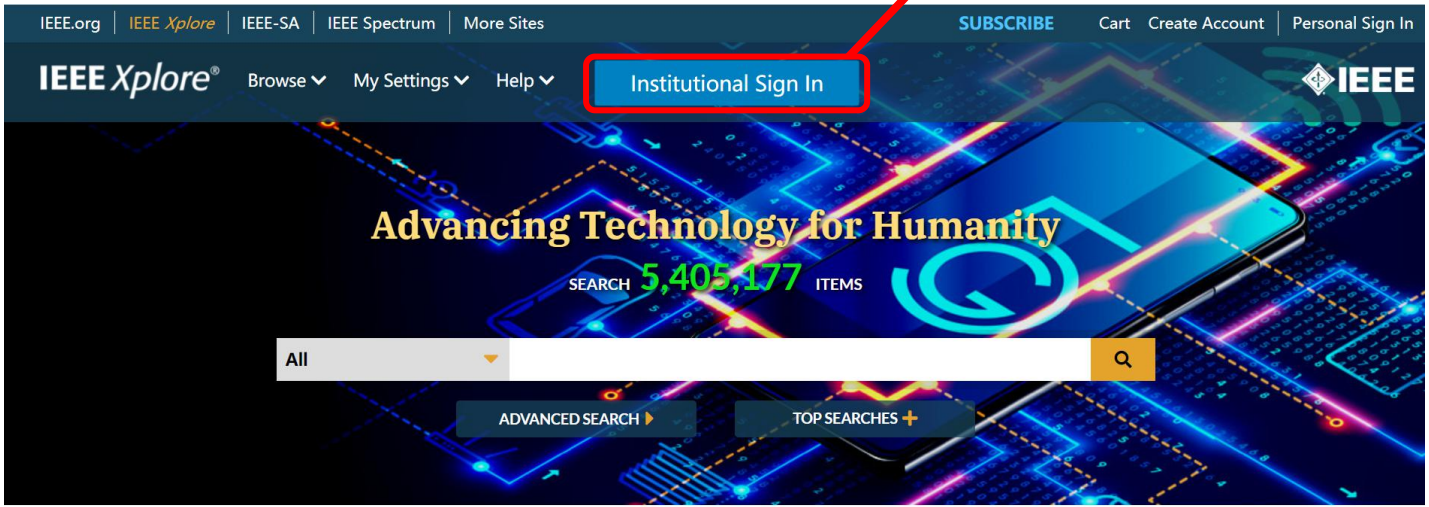

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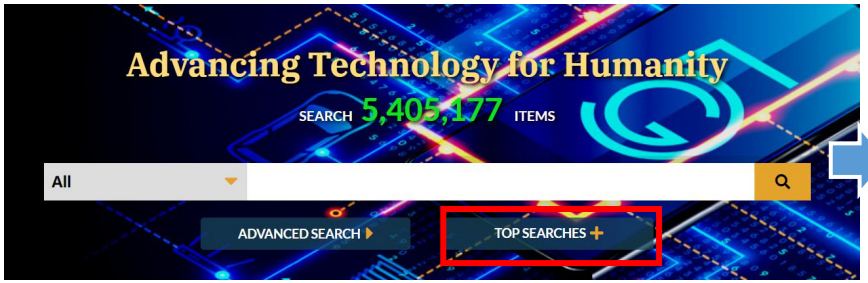

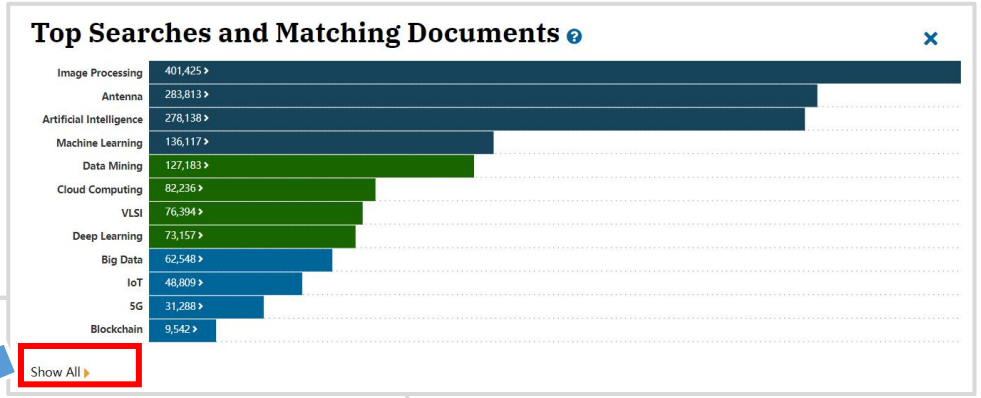

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Raymond W. Yeung (Fellow, IEEE) was born in Hong Kong in June 1962. He received the B.S., M.Eng., and Ph.D. degrees in electrical engineering from Cornell University, Ithaca, NY, USA, in 1984, 1985, and 1988, respectively.,He was on leave at the École Nationale Supérieure des Télécommunications, Paris, France, in Fall 1986. He was a Member of Technical Staff of AT&T Bell Laboratories from 1988 to 1991. Since 1991, he has been with The Chinese University of Hong Kong, where he is currently a Choh-Ming Li Professor of information engineering and the Co-Director of the Institute of Network Coding. He has held visiting positions at Cornell University, Nankai University, Bielefeld University, the University of Copenhagen, the Tokyo Institute of ... Show More

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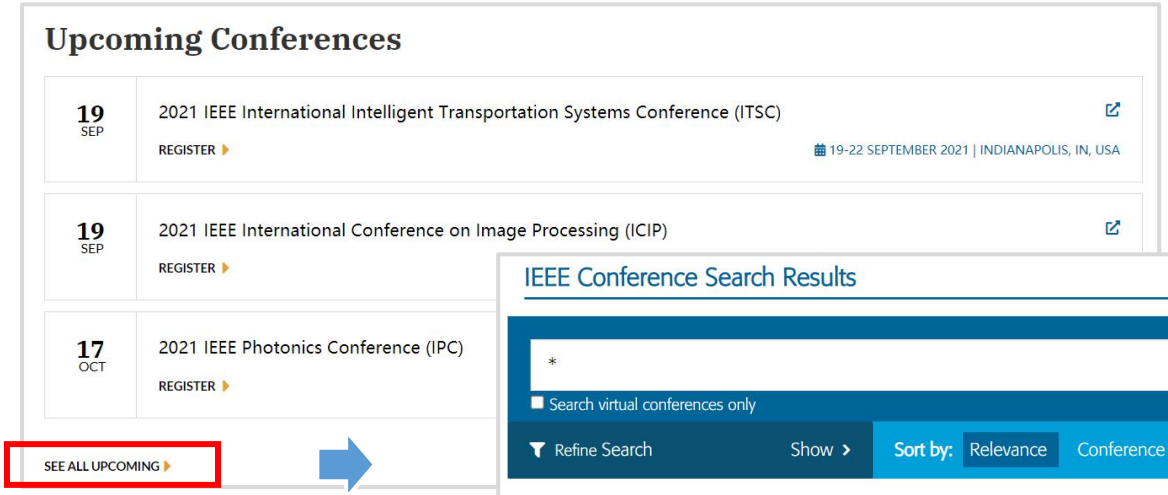

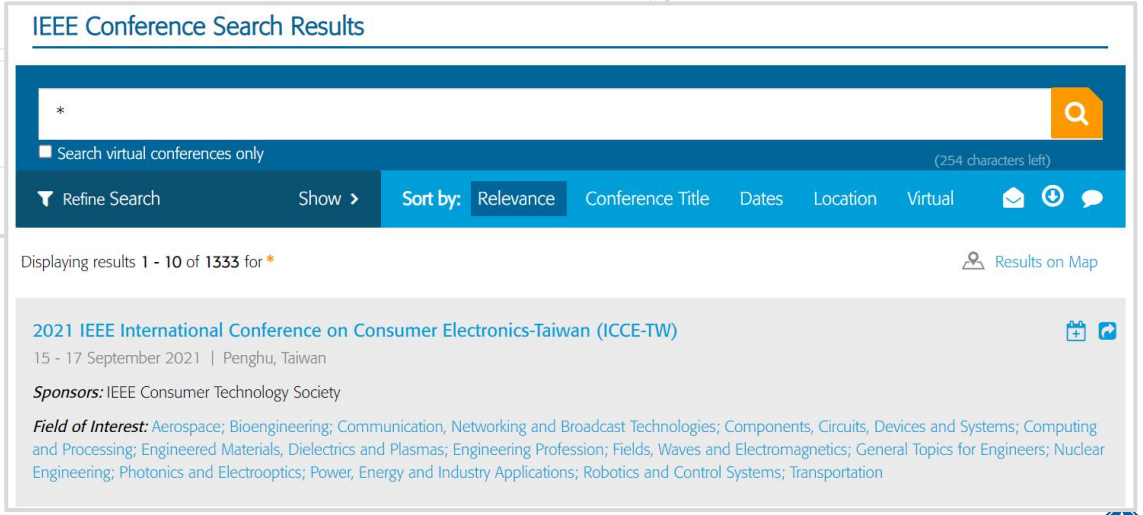

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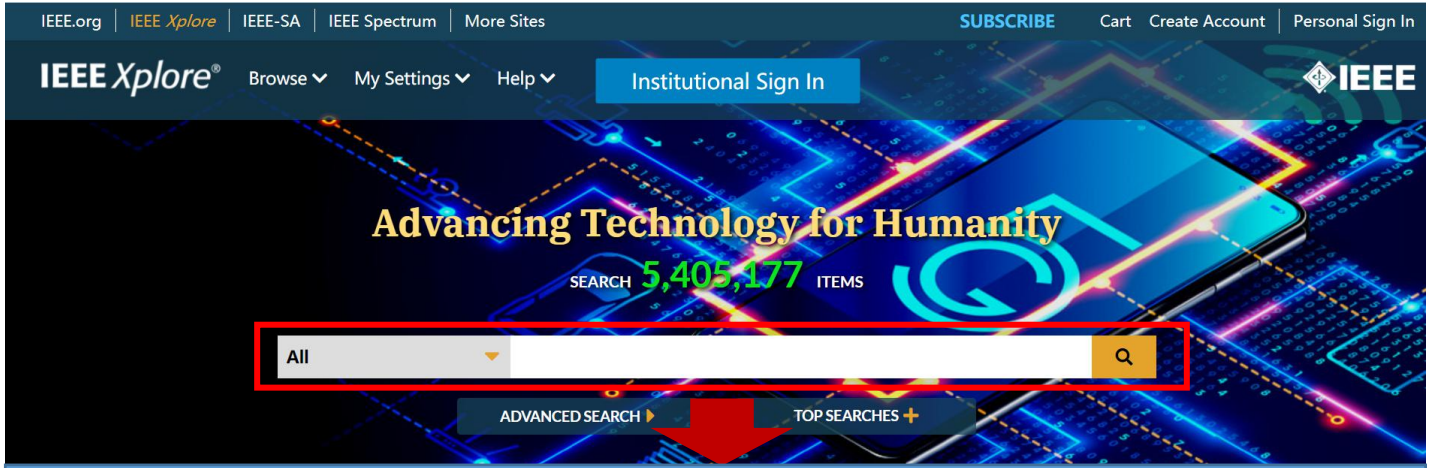

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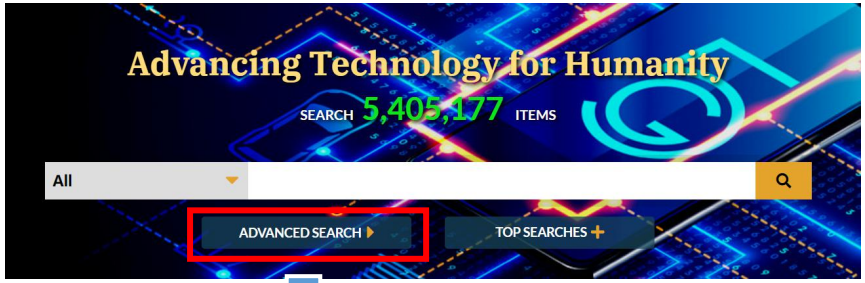

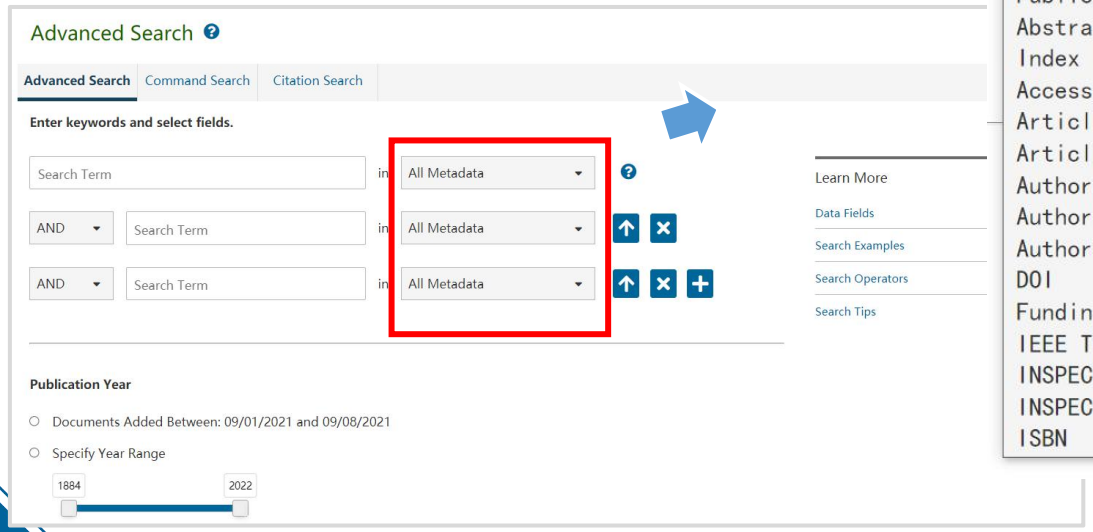

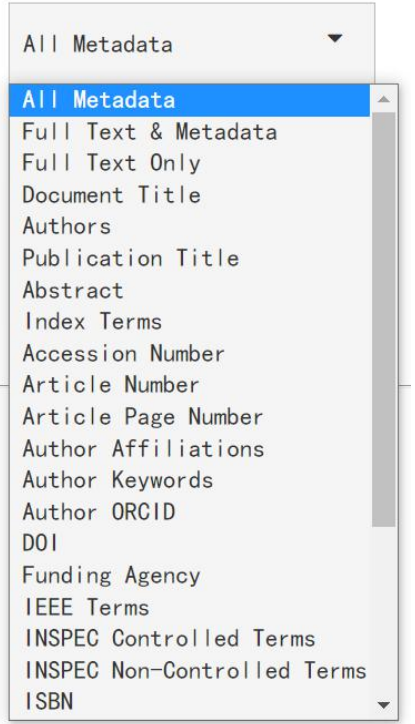

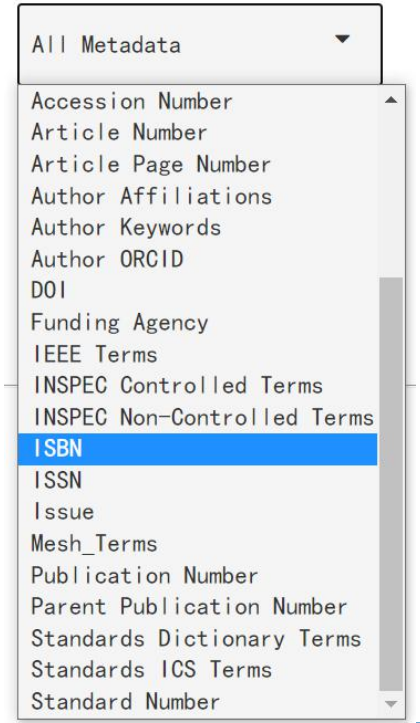

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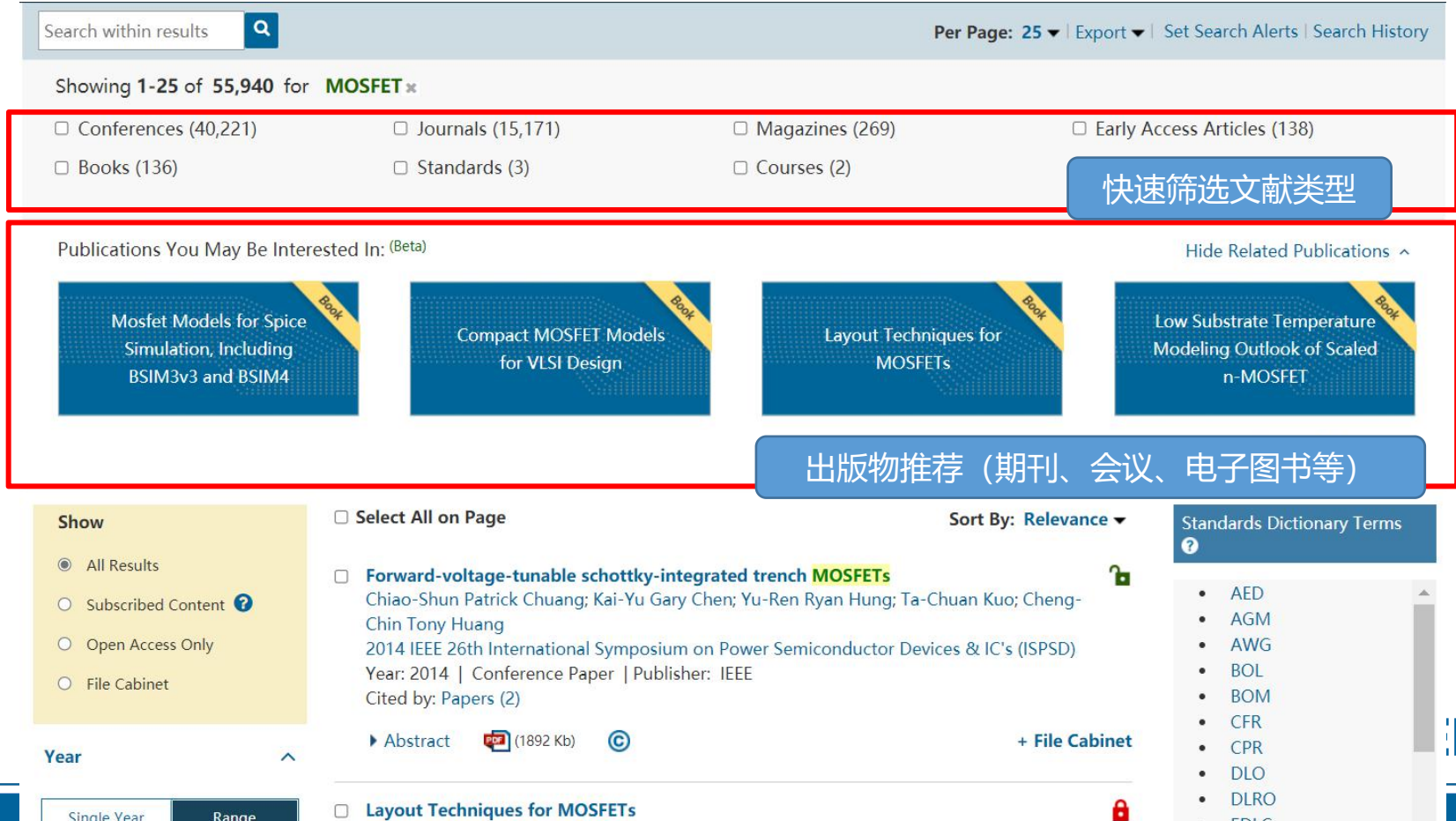

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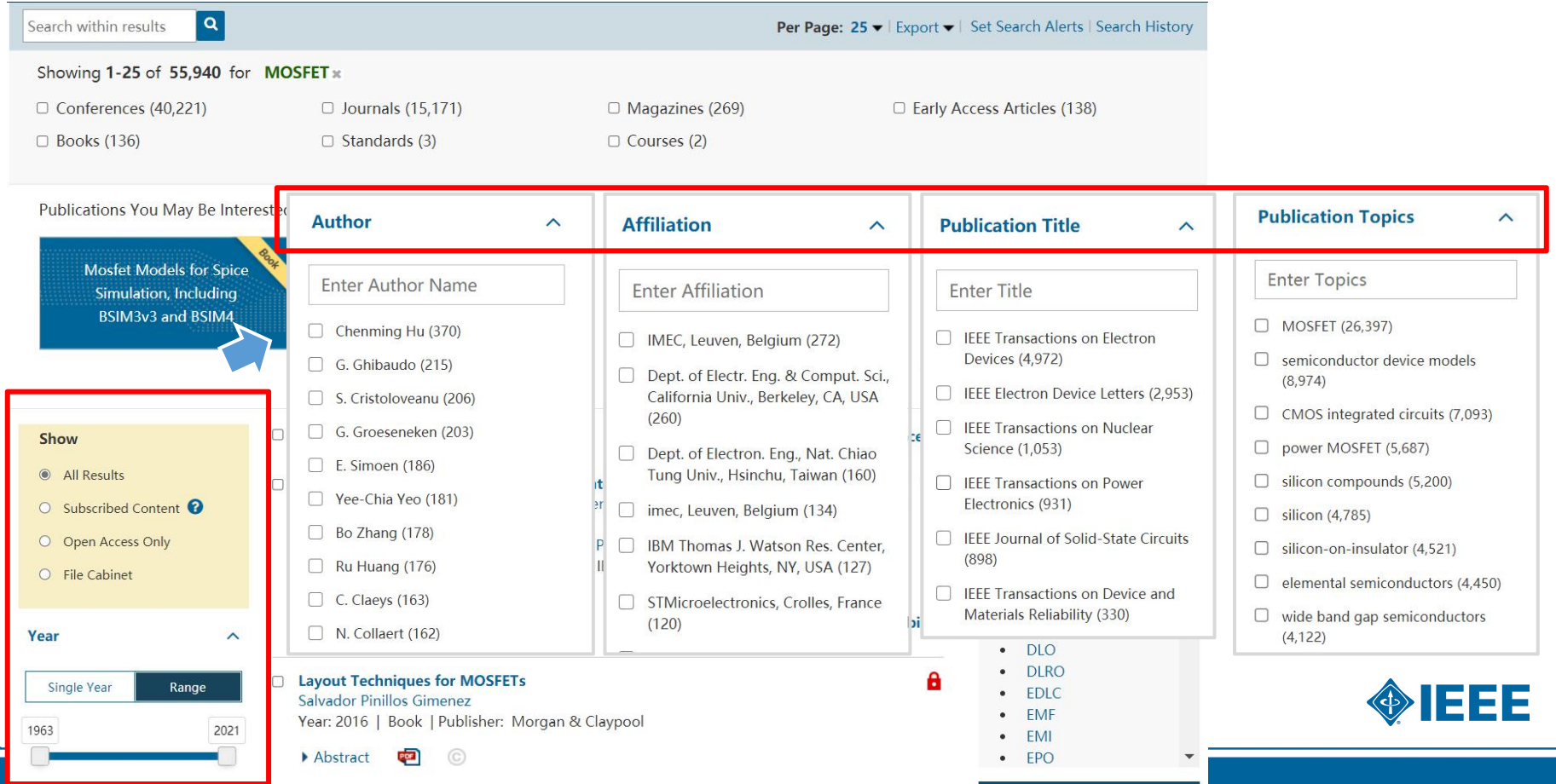

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T. Tang; C. Burkhart

IEEE Transactions on Dielectrics and Electrical Insulation

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The ultra-fast switching of power MOSFETs, in about 1 ns, is very challen... the parasitic inductance that is intrinsic to commercial packages used fo... drivers. Parasitic gate and source inductance not only limit the voltage ri... internal gate structure but can also cause the gate voltage to oscillate. This paper describes a hybrid approach that substantially reduces the parasitic inductance between the driver and MOSFET gate, as well as between the MOSFET source and its external connection. A flip-chip assembly is used to directly attach a die-form power MOSFET and driver on a PCB. The parasitic inductances are significantly reduced by eliminating bond wires and minimizing lead length. The experimental results demonstrate ultra-fast switching of the power MOSFET with excellent control of the gate-source voltage.

推荐文献

Published in: IEEE Transactions on Dielectrics and Electrical Insulation (Volume: 16 , Issue: 4, August 2009)

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SECTION I. Introduction

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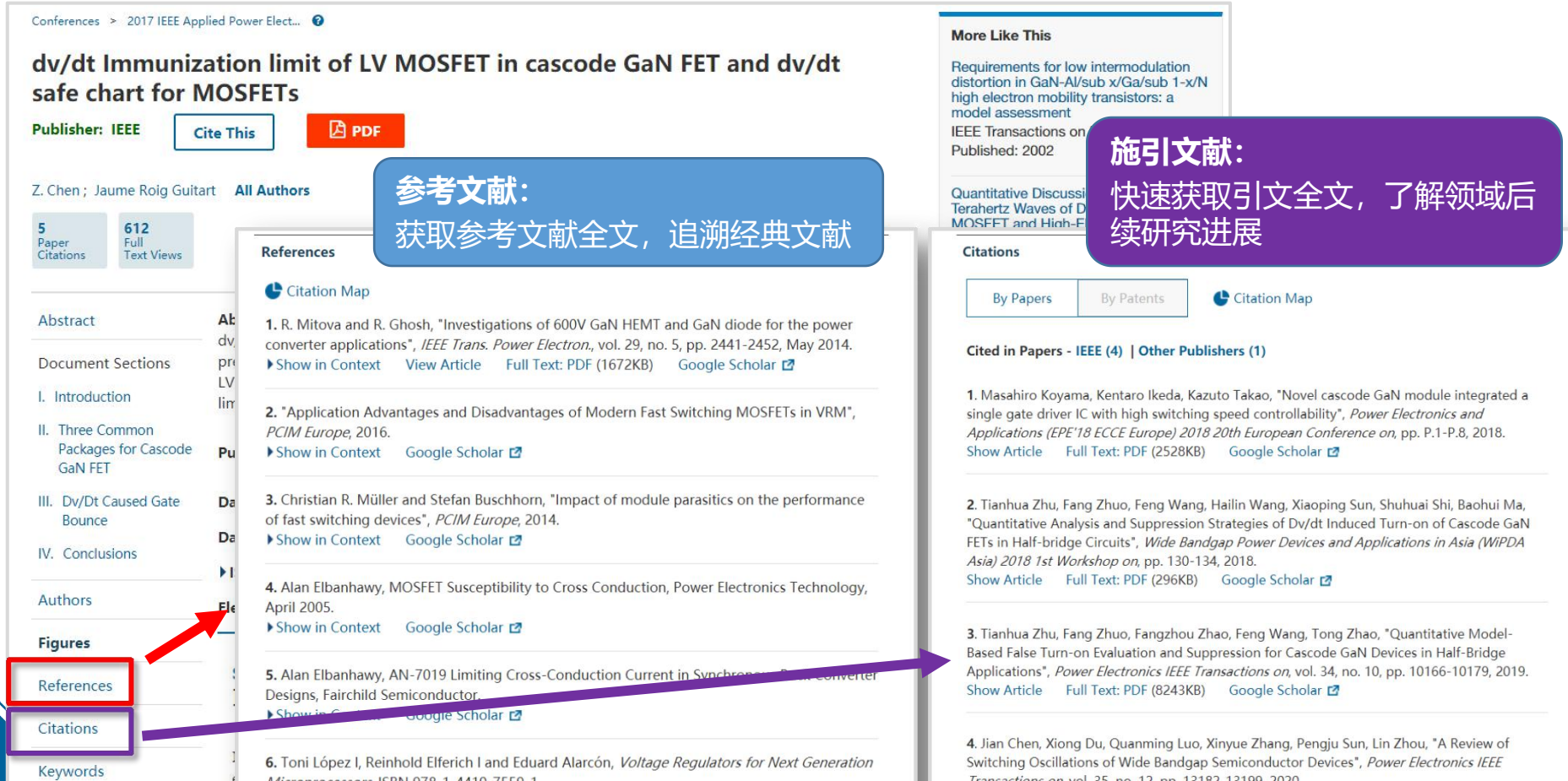

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Department of Electrical Engineering and Computer Science, University of California, Berkeley, Berkeley, CA, USA

了解作者详情

Chenming Hu (F' 03) is the TSMC Distinguished Professor Emeritus of University of California Berkeley, Berkeley, CA, USA. He is a Former Chief Technology Officer of TSMC. He is a Board Director of SanDisk Inc., and of the non-profit Friends of Children with Special Needs. He is well known for his work on the 3-D transistor, FinFET, which can be scaled to single digit nanometers. He has developed widely used IC reliability models and led the research of BSIM—the first industry—standard SPICE model used by most IC companies to design CMOS products since 1996. He was a recipient of the IEEE Andrew Grove Award, the Solid State Circuits Award and Nishizawa Medal, the Kaufman Award of the EDA industry, the University Research Award of the U.S. Semiconductor Industry Association, and the UC Berkeley's Highest Honor for teaching—the Berkeley Distinguished Teaching Award.

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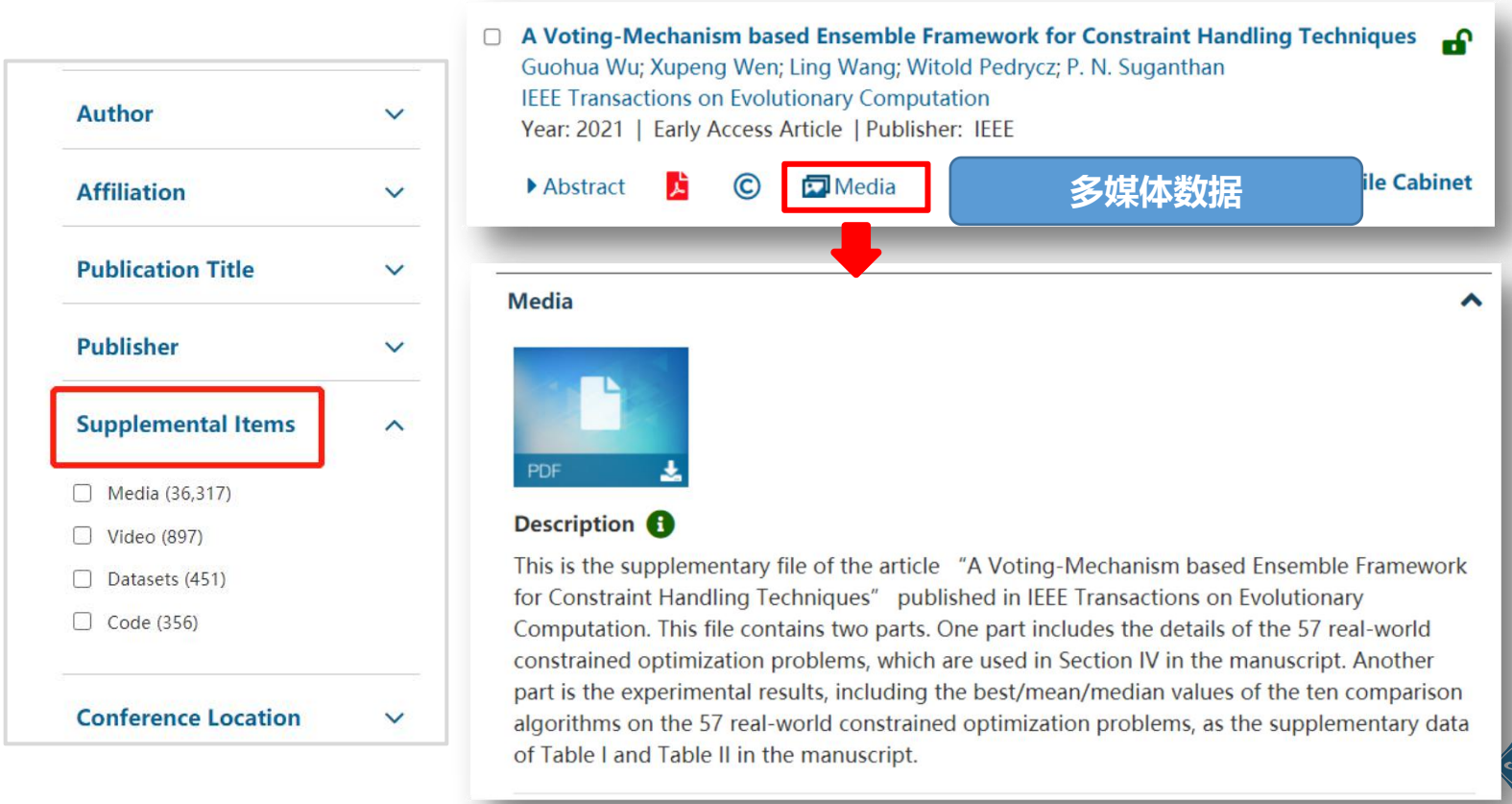

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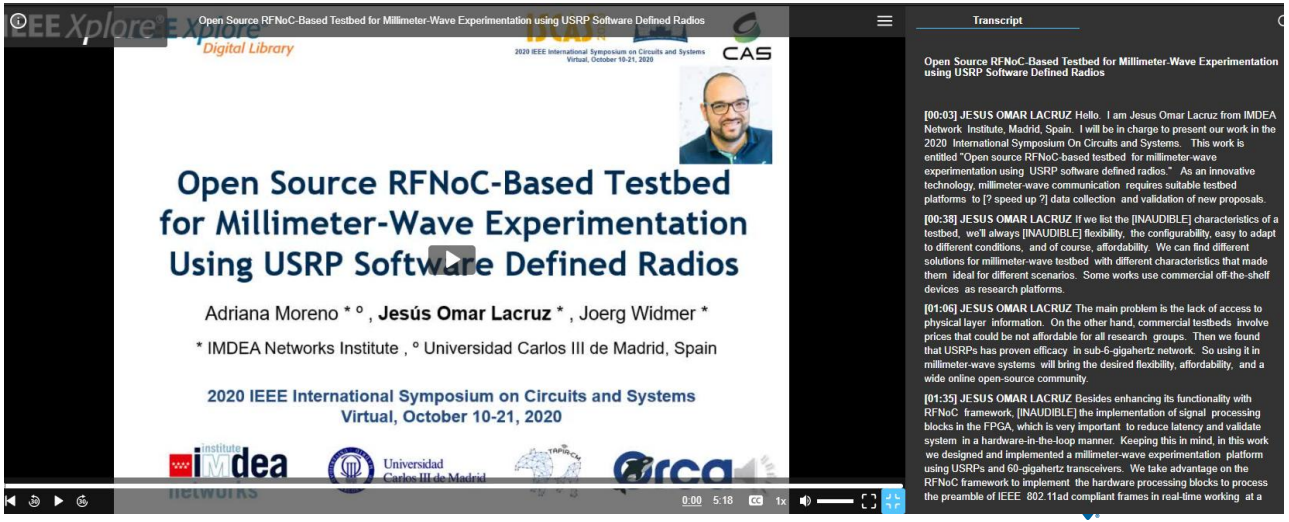

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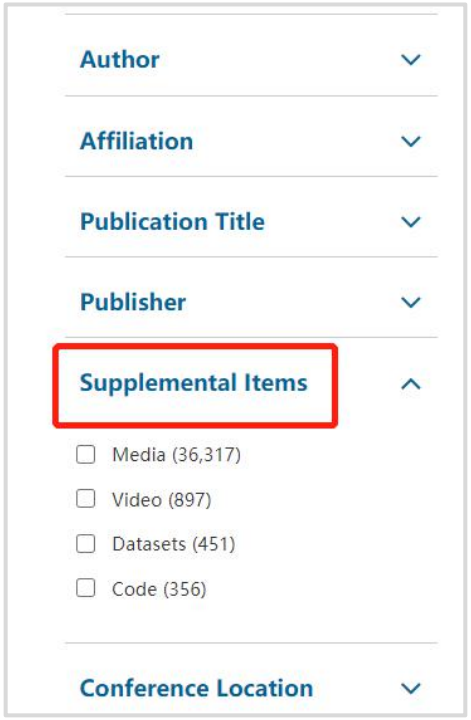

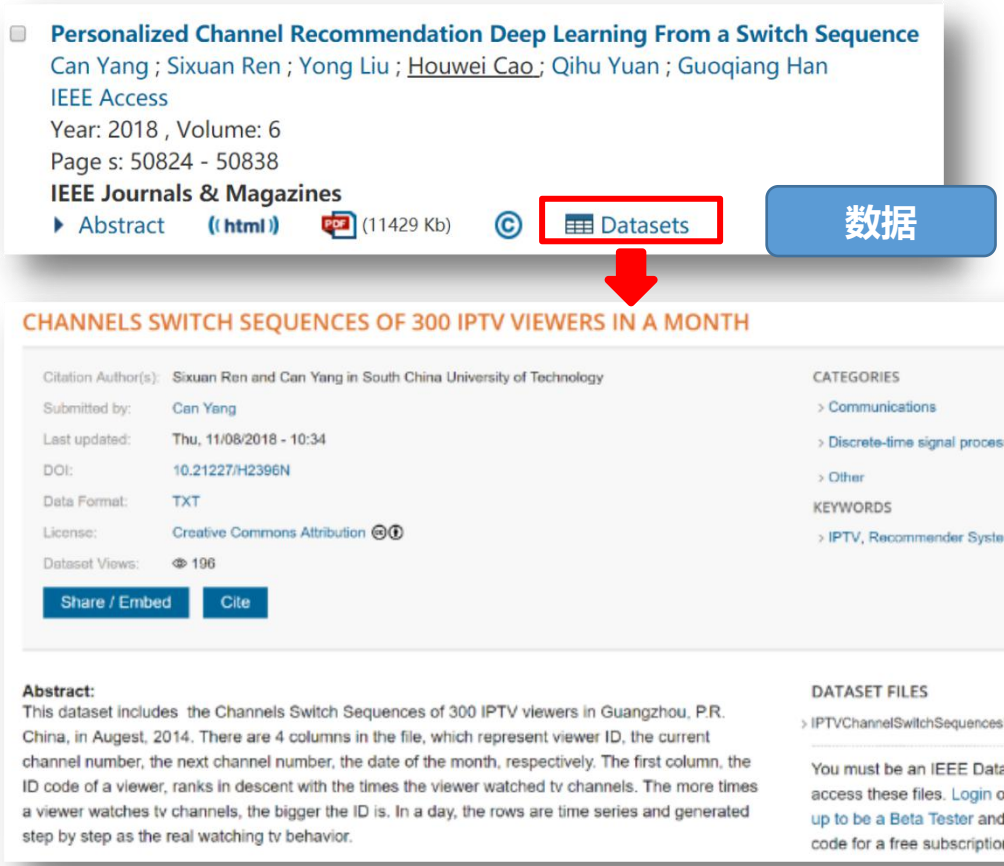

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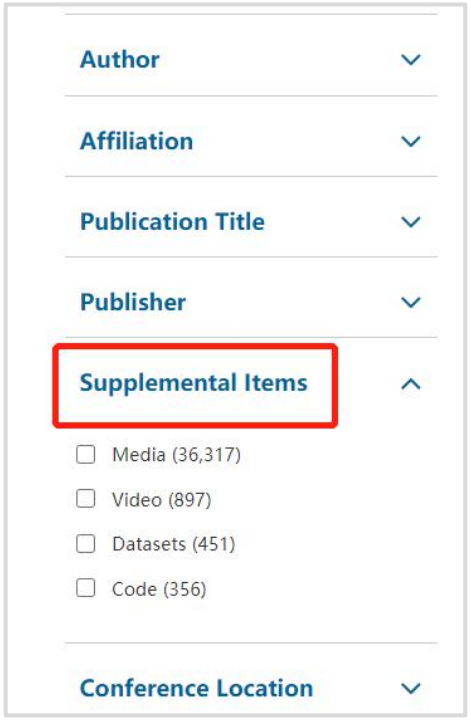

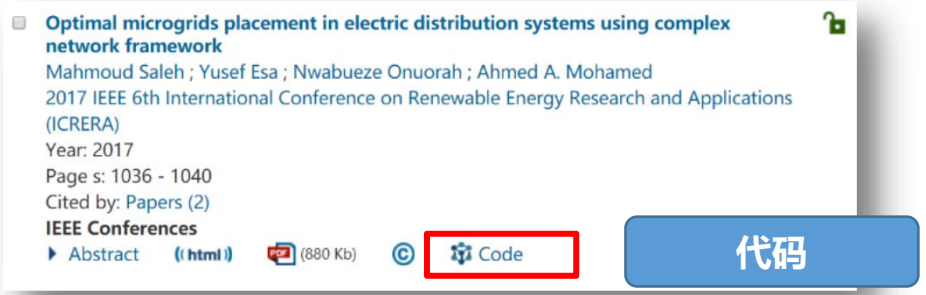

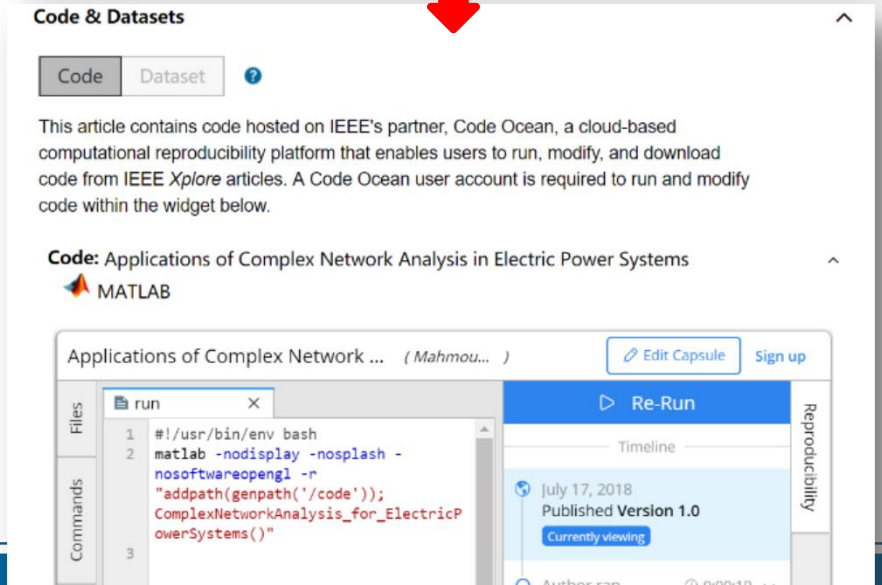

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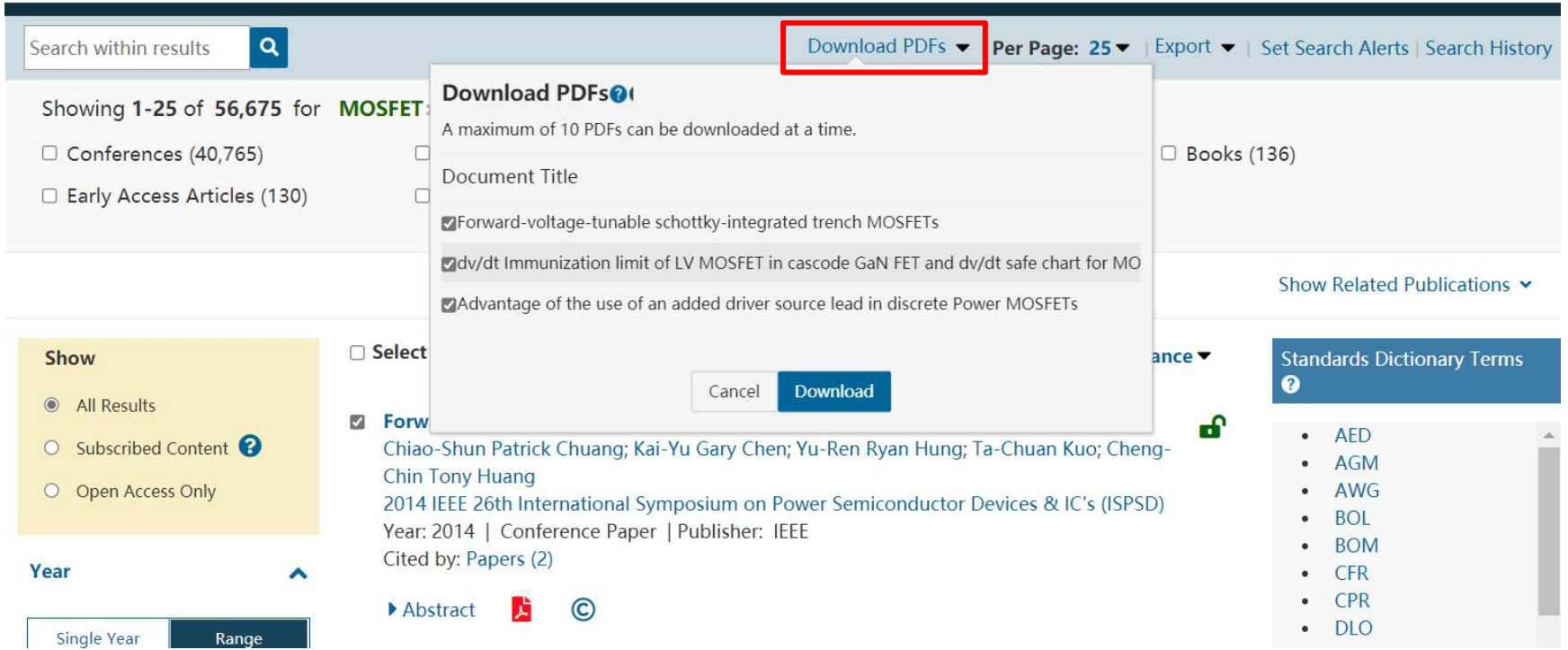
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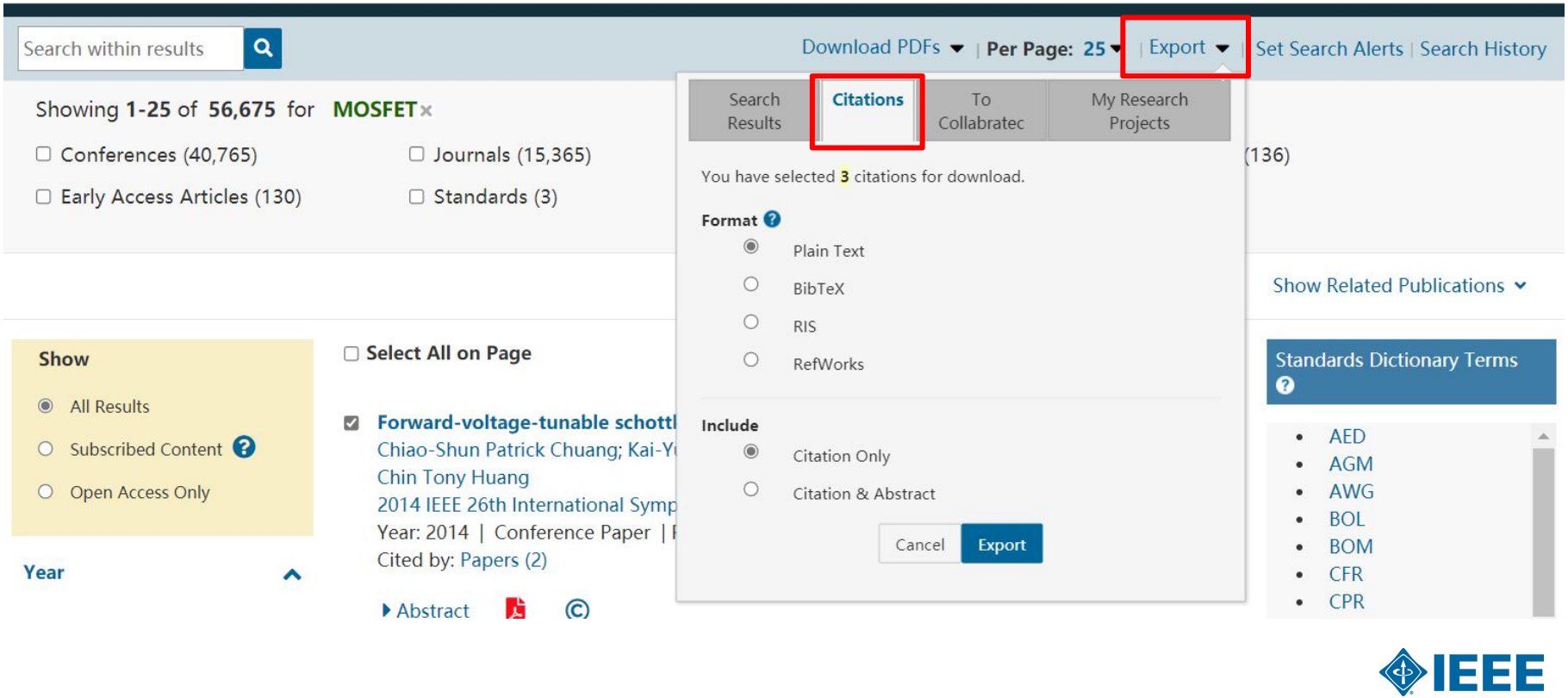
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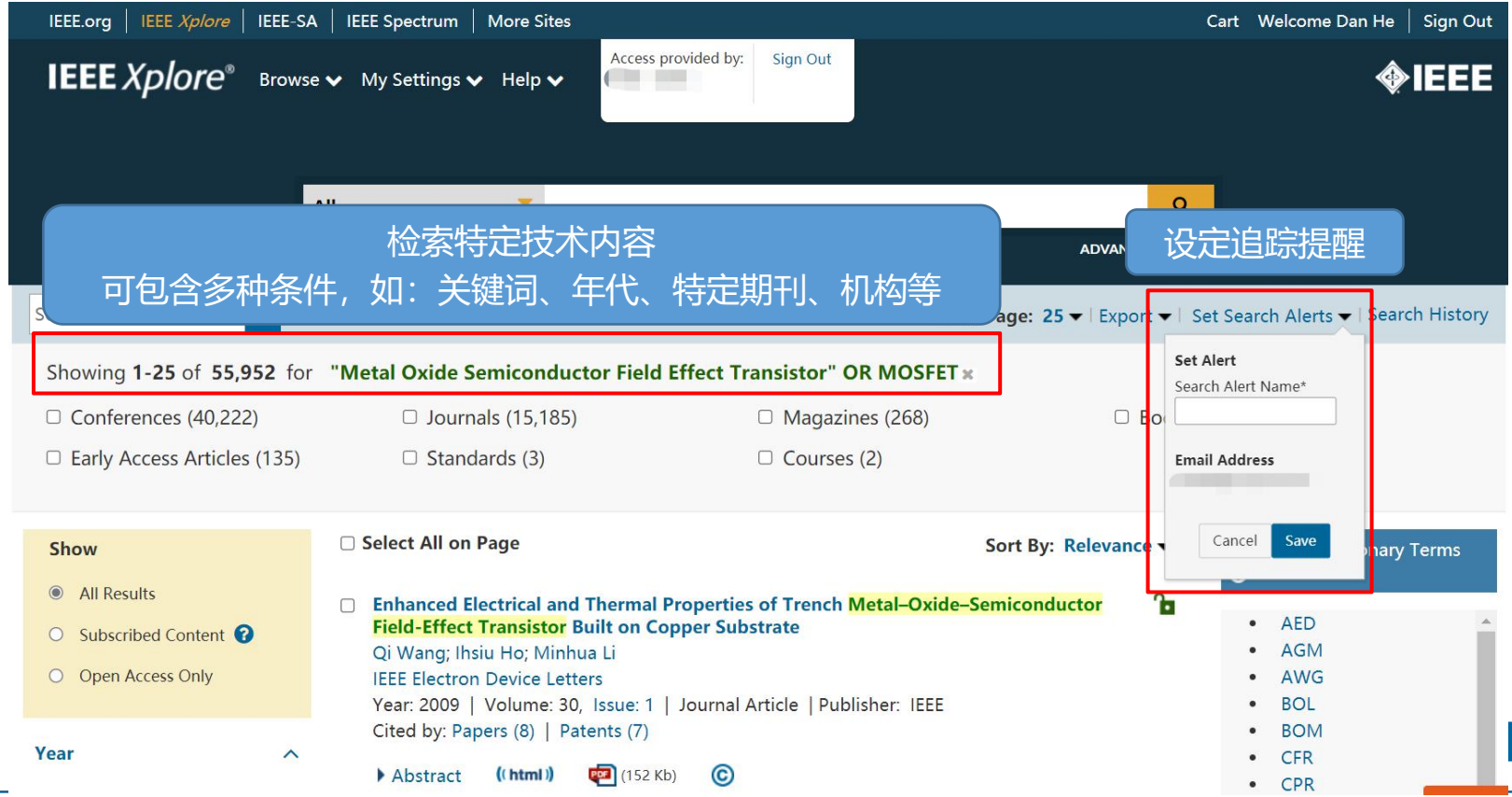

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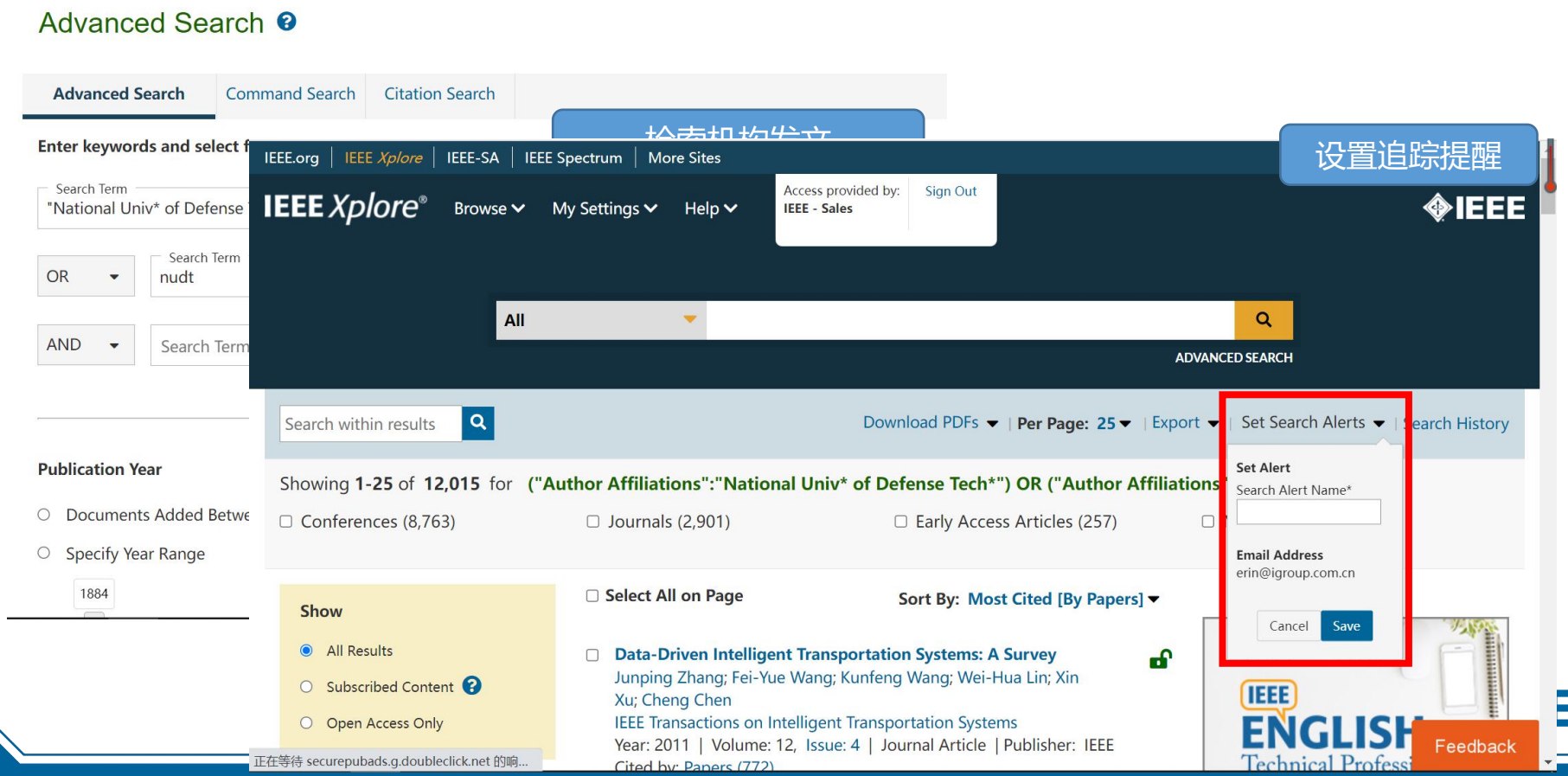

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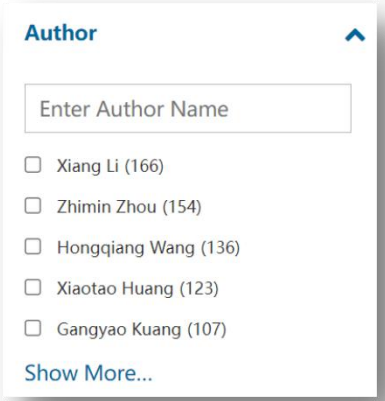

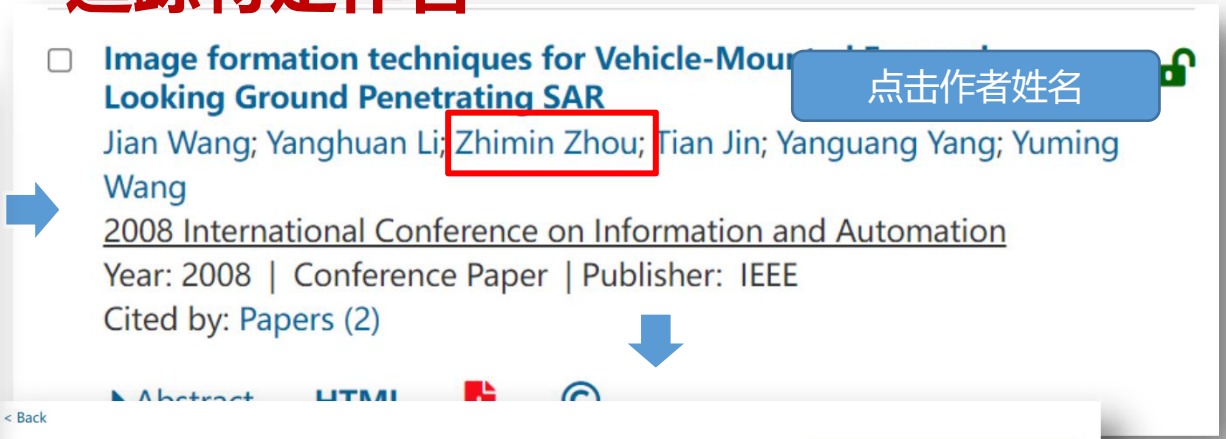

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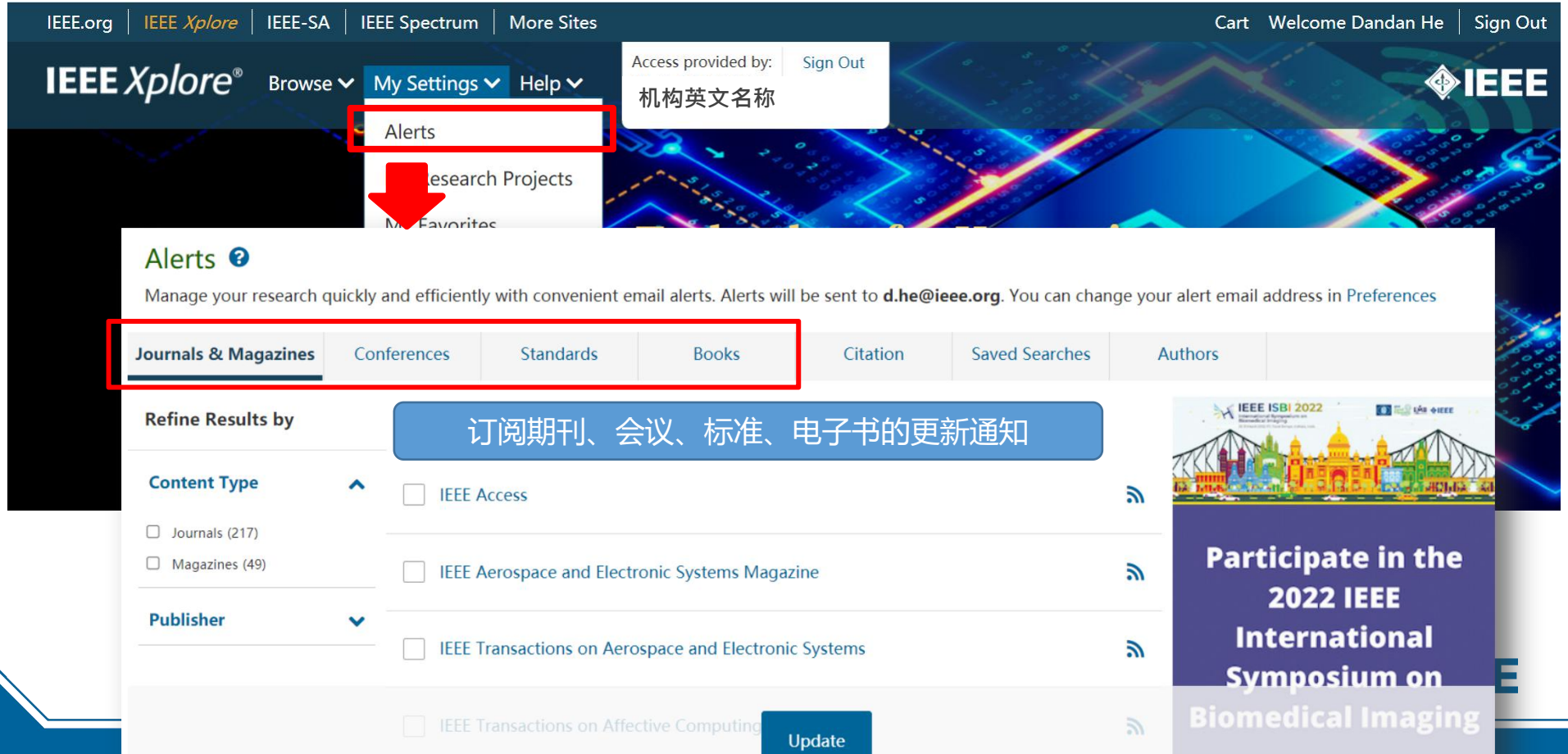

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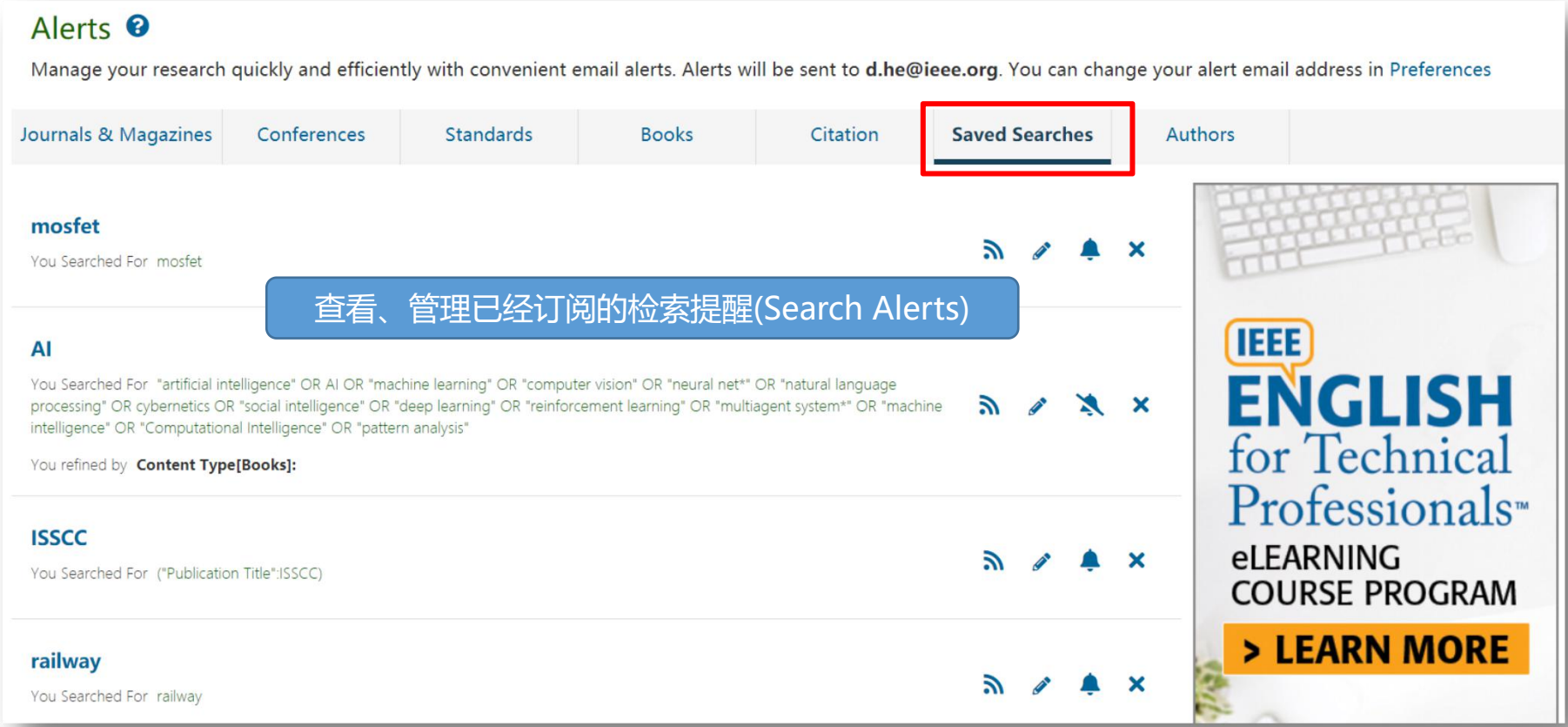


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